


Helping Customers Innovate, Improve & Grow



Description

The VS-751 is a SAW based voltage controlled oscillator that operates at the fundamental frequencies of the internal SAW filters. These SAW filters are high-Q quartz devices that enable the circuit to achieve low phase jitter performance over a wide operating temperature range. The dual oscillator is housed in a hermetically sealed leadless surface mount package offered on tape and reel. It has a frequency select function that enables either "Frequency 1" or "Frequency 2."

Features

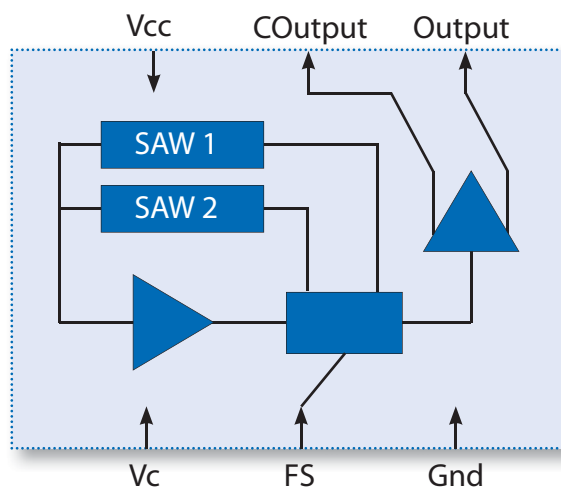
- 5x7.5x2.5 mm Package
- Output frequencies from 500MHz to 850MHz
- 3.3V operation
- Low Jitter <0.25 ps-rms across 50kHz to 80MHz
- LV-PECL configuration with fast transition times
- Complementary outputs
- Frequency select
- Patent pending technology
- Product is free of lead and compliant to EC RoHS directive 

Applications

PLL circuits for clock smoothing and frequency translation

Description	Standard
• 1-2-4 Gigabit Fibre Channel	INCITS 352-2002
• 10 Gigabit Fibre Channel	INCITS 364-2003
• 10GbE LAN / WAN	IEEE 802.3ae
• OC-192	ITU-T G.709
• SONET / SDH	GR-253-CORE Issue4
• Synchronous Ethernet	ITU-T.8262

Block Diagram

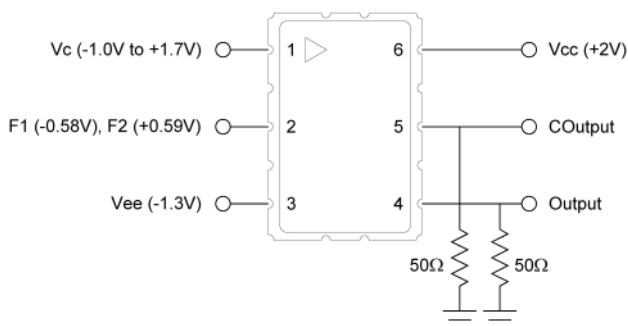


Performance Specifications

Electrical Performance						
Parameter	Symbol	Min	Typical	Maximum	Units	Notes
Supply						
Voltage	V_{CC}	2.97	3.3	3.63	V	2,3
Current (No Load)	I_{CC}		55	70	mA	3
Frequency						
Nominal Frequency	f_N		500 - 850		MHz	1,2,3
Absolute Pull Range	APR	± 50			ppm	1,2,3,8
Linearity	Lin		± 5		%	2,4,8
Gain Transfer (See pg 5)	K_V		+405		ppm/V	2,8
Temperature Stability	f_{STAB}		± 100		ppm	1,6
Transition Time			4		μsec	6
Outputs						
Mid Level		$V_{CC}-1.4$	$V_{CC}-1.3$	$V_{CC}-1.2$	V	1,3
Swing		550	650	950	mV-pp	2,3
Current	I_{OUT}			20	mA	6
Rise Time	t_R		250	400	ps	5,6
Fall Time	t_F		250	400	ps	5,6
Symmetry	SYM	45	50	55	%	2,3
Spurious Suppression		50	60		dBc	6
Jitter (See pg 5)	ϕJ		0.130	0.250	ps-rms	6,7
Control Voltage						
Input Impedance	Z_C		100		k Ω	6
Modulation Bandwidth	BW		500		kHz	6
Operating Temperature	T_{OP}	-40		85	$^{\circ}\text{C}$	1,3
Package Size		5.0 x 7.5 x 2.5			mm	

- 1] See standard frequencies and ordering information (Pg 7).
- 2] Parameters are tested with production test circuit below (Fig 1).
- 3] Parameters are tested at ambient temperature with test limits guardbanded for specified operating temperature.
- 4] Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
- 5] Measured from 20% to 80% of a full output swing (Fig 2).
- 6] Not tested in production, guaranteed by design, verified at qualification.
- 7] Integrated across 50kHz to 80MHz, per GR-253-CORE Issue3.
- 8] Tested with $V_C = 0.3V$ to $3.0V$.

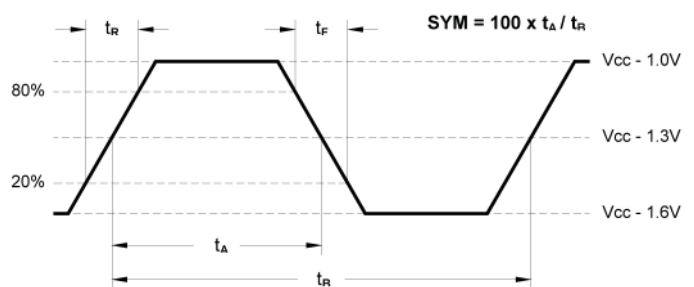
Fig 1: Test Circuit



Test Circuit Notes:

- 1] To permit 50 Ω easurement of outputs, all DC inputs are biased down 1.3V.
- 2] All voltage sources contain bypass capacitors to minimize supply noise.
- 3] 50 Ω terminations are within test equipment.

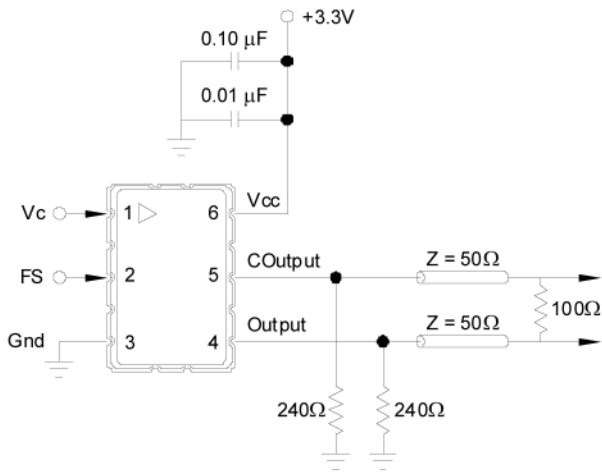
Fig 2: 10K LV-PECL Waveform



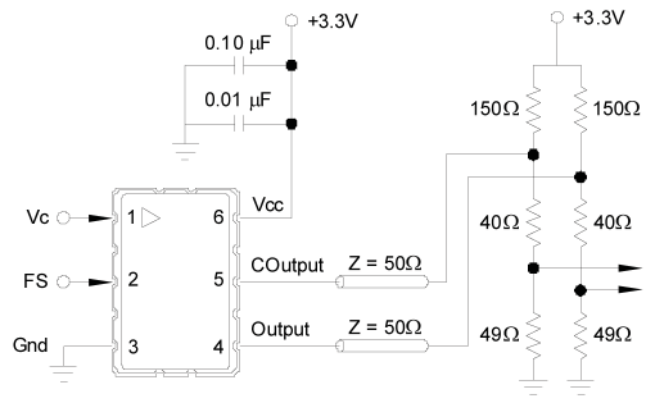
Absolute Maximum Ratings			
Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Voltage	V_C	0 to V_{CC}	V
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature / Duration	T_{PEAK} / t_p	260 / 40	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods may adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet. Permanent damage is also possible if any device input (V_C or FS) draws greater than 100mA.

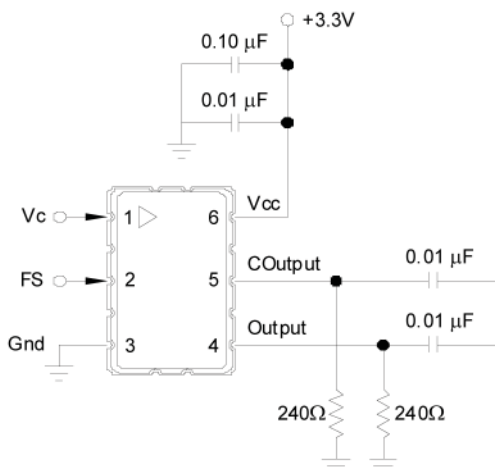
Suggested Output Load Configuration



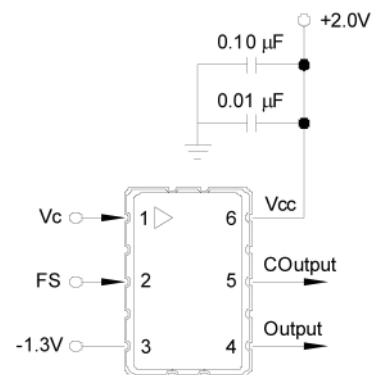
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.

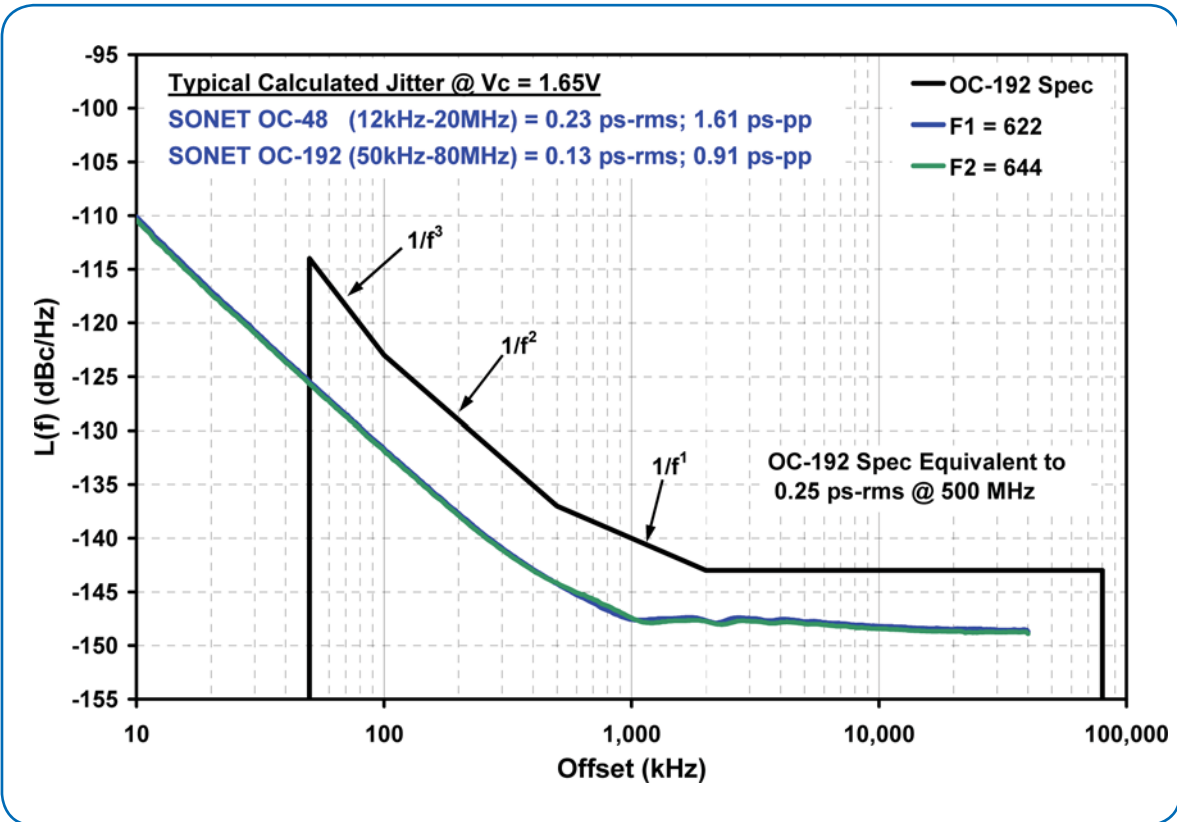
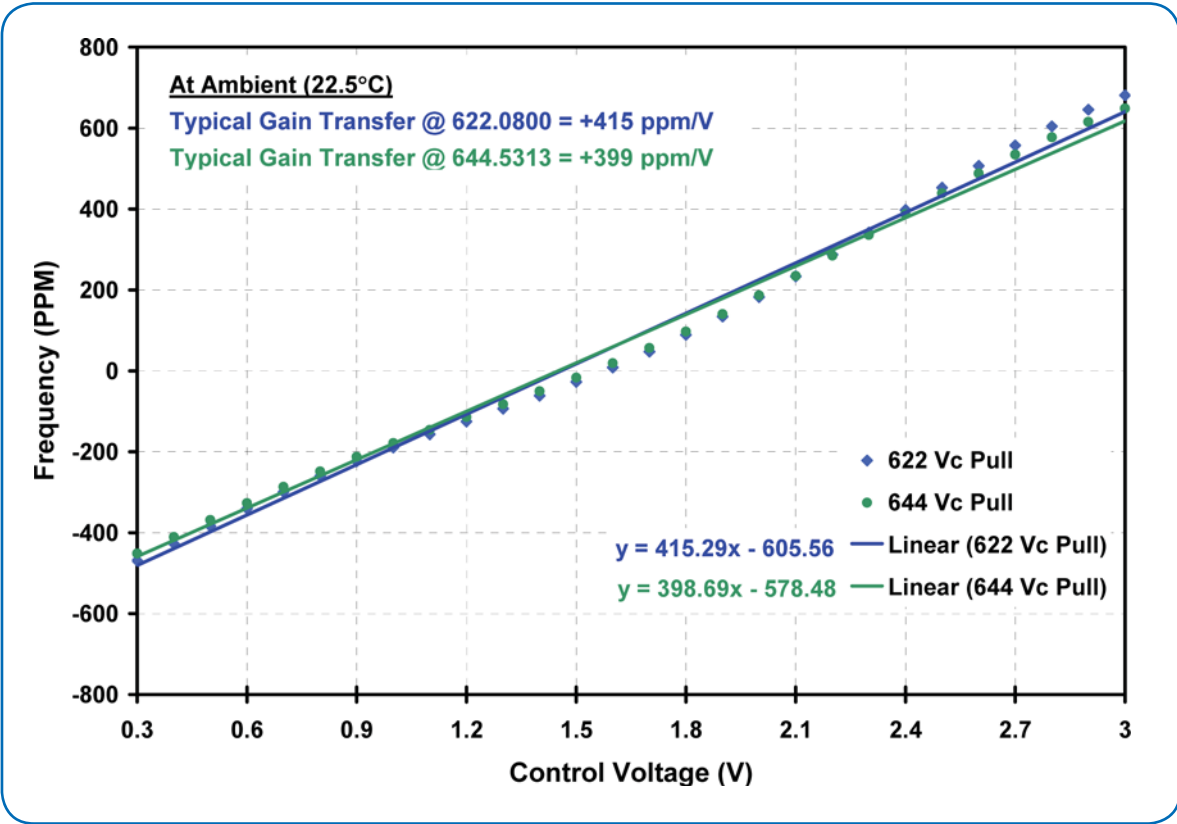


Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplies as shown. Similar to Figure 1.

Typical Characteristics



Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-751 family is capable of meeting the following qualification test at right:

Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

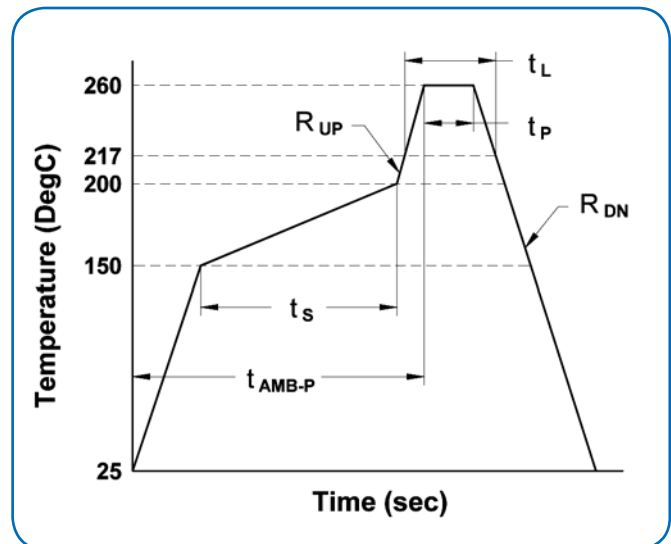
Although ESD protection circuitry has been designed into the VS-751 proper precautions should be taken when handling and outting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	Minimum	Conditions
Human Body Model	1500V	MIL-STD-883, Method 3015
Charged Device Model	1000V	JEDEC, JESD22-C101

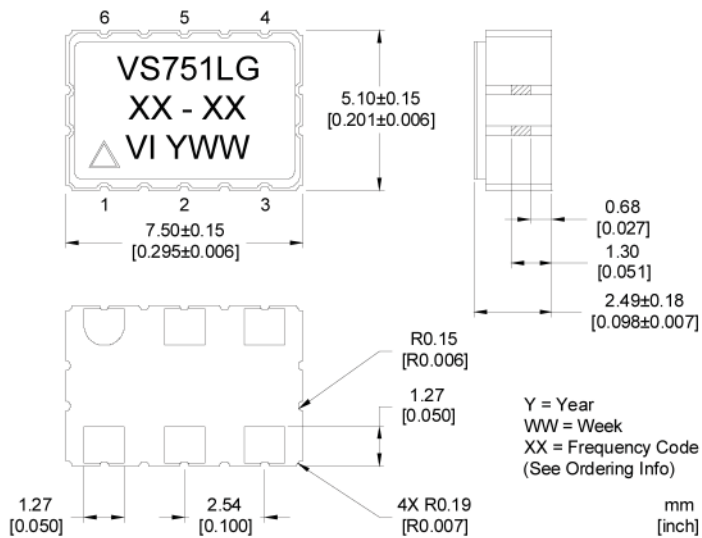
Reflow Profile (IPC/JEDEC J-STD-020C)		
Parameter	Symbol	Value
PreHeat Time	t_s	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-751 device is hermetically sealed so an aqueous wash is not an issue.

Terminal Plating: Electroless Gold Plate over Nickel Plate

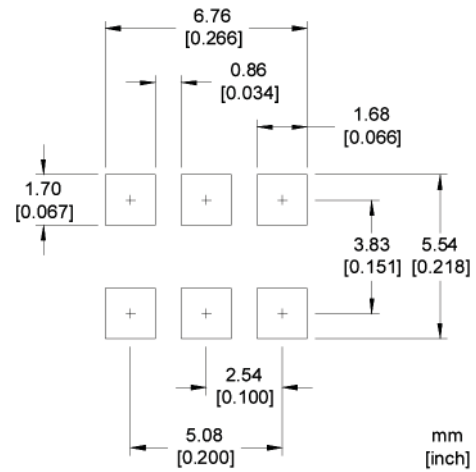


Outline Drawing



Suggested Pad Layout

Dimensions in inches (mm)



Pin Out

Pin	Symbol	Function
1	V_C	VCSO Control Voltage
2	FS	Frequency Select (see control logic)
3	Gnd	Case and Electrical Ground
4	Output	VCSO Output
5	COutput	VCSO Coplementary Output
6	V_{CC}	Power Supply Voltage (3.3V ± 10%)

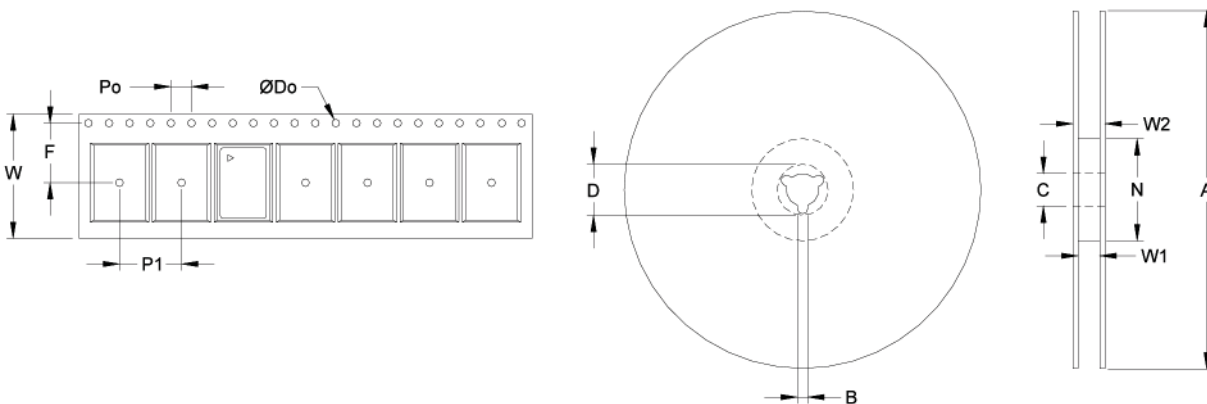
Marking Key

Position 6	Position 7
L = LFF	G = GNN
	H = HNN

Control Logic (LV-CMOS)

FS	Operation
0	F1
1	F2

Tape & Reel (EIA-481-2-A)



Tape Dimensions (mm)

Reel Dimensions (mm)

Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VS-751	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

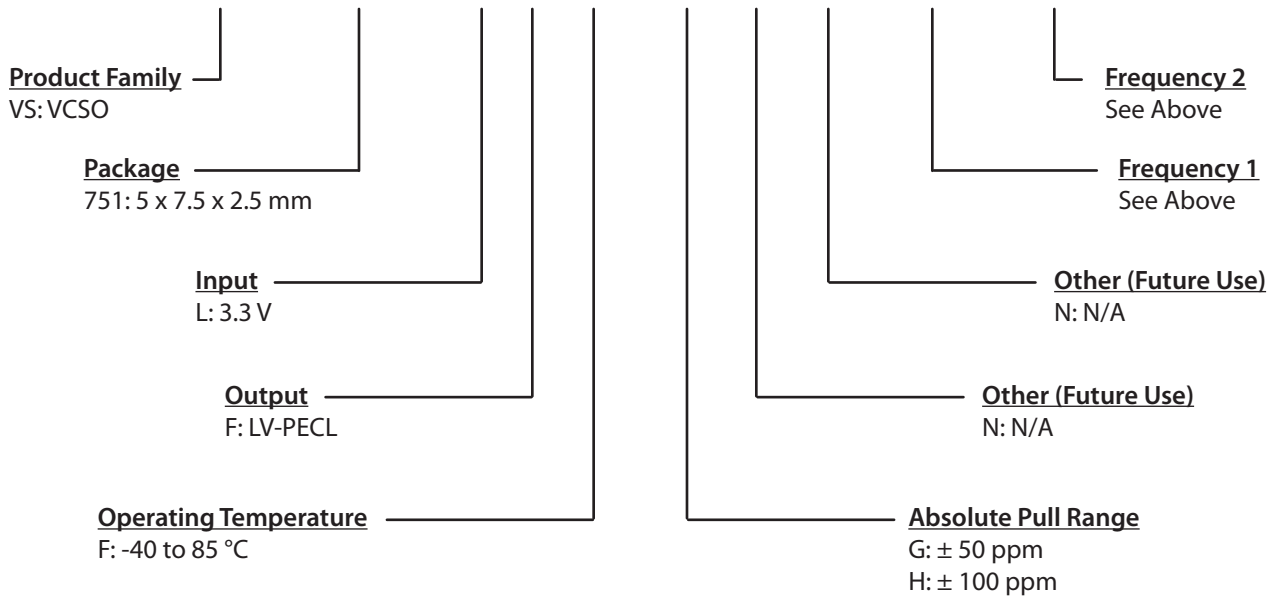
Standard Frequencies (MHz)

531.250000 P8	569.196400 P9	614.400000 RG	622.080000 P2	624.693800 PD	625.000000 P3
627.329600 P7	629.987800 PA	644.531250 P4	657.421875 PB	666.514286 P5	669.326582 R3
669.642900 R1	672.156250 TX	672.162712 R5	687.700000 TV	690.569196 R4	693.482991 R6
693.750000 R8	696.421478 V1	696.421875 TY	704.380600 TG	707.352700 TC	707.500000 V2
712.520000 TW	737.280000 TL	777.600000 T4	805.664100 TA		

- Other frequencies available upon request, please contact VI for details.
- Frequency 1 must be lower than frequency 2. Not all combinations are available.

Ordering Information

VS - 751 - L F F - H N N - P2 - P2



Example: VS-751-LFF-HNN-P2-P4

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Revision History

Revision History		
Date	Approved	Description
09Jan2006	JM	Original Issue
07Dec2006	JM	Added TG frequency code
12Nov2009	BW	Added the following frequency codes: RG, TL, TV, TX, TW, TY, V1, V2