

25W Power Packaged Transistor

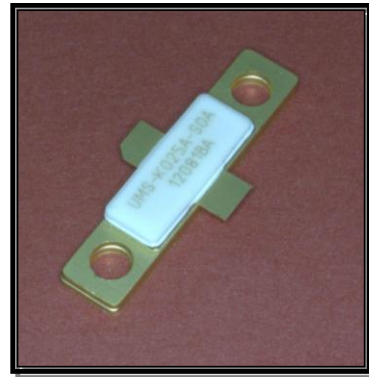
GaN HEMT on SiC

Description

The CHK025A-SOA is an unmatched packaged Gallium Nitride High Electron Mobility Transistor. It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication.

The CHK025A-SOA is developed on a 0.5 μ m gate length GaN HEMT process. It requires an external matching circuitry.

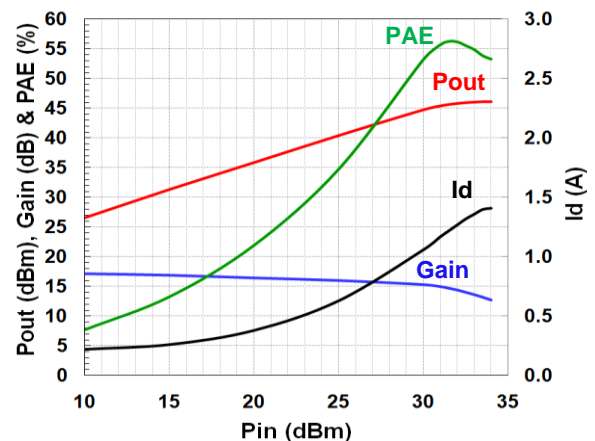
The CHK025A-SOA is available as a ceramic-metal flange power package providing low parasitic and low thermal resistance.



Main Features

- Wide band capability: up to 5GHz
- Pulsed and CW operating modes
- High power: > 25W
- High Efficiency: up to 70%
- DC bias: $V_{DS} = 50V$ @ $I_{D,Q} = 200mA$
- MTTF > 10^6 hours @ $T_j = 200^\circ C$
- RoHS Flange Ceramic package

$V_{DS} = 50V$, $I_{D,Q} = 200mA$, Freq=4GHz
Pulsed mode



Intrinsic performances of the packaged device

Main Electrical Characteristics

$T_{case} = +25^\circ C$, Pulsed mode, $F = 4GHz$, $V_{DS} = 50V$, $I_{D,Q} = 200mA$

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	15	17		dB
P_{SAT}	Saturated Output Power	30	38		W
PAE	Max Power Added Efficiency	55	60		%
G_{PAE_MAX}	Associated Gain at Max PAE		13		dB

Recommended DC Operating Ratings

T_{case}= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _{DS}	Drain to Source Voltage	20		50	V	
V _{GS_Q}	Gate to Source Voltage		-1.9		V	V _D =50V, I _{D_Q} =200mA
I _{D_Q}	Quiescent Drain Current		0.2	0.65	A	V _D =50V
I _{D_MAX}	Drain Current		1.3	⁽¹⁾	A	V _D =50V, Compressed mode
I _{G_MAX}	Gate Current (forward mode)		0	16	mA	Compressed mode
T _{J_MAX}	Junction temperature			200	°C	

⁽¹⁾ Limited by dissipated power

DC Characteristics

T_{case}= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _P	Pinch-Off Voltage	-3	-2	-1	V	V _D =50V, I _D = I _{DSS} /100
I _{D_SAT}	Saturated Drain Current		5.4 ⁽¹⁾		A	V _D =7V, V _G =2V
I _{G_leak}	Gate Leakage Current (reverse mode)	-2			mA	V _D =50V, V _G =-7V
V _{BDS}	Drain-Source Break-down Voltage		200		V	V _G =-7V, I _D =20mA
R _{TH}	Thermal Resistance		3.7		°C/W	

⁽¹⁾ For information, limited by I_{D_MAX}, see on Absolute Maximum Ratings

RF Characteristics (CW)

T_{case}= +25°C, CW mode, F = 4GHz, V_{DS}=50V, I_{D_Q}=200mA

Symbol	Parameter	Min	Typ	Max	Unit
G _{SS}	Small Signal Gain	14	16	-	dB
P _{SAT}	Saturated Output Power	28	35	-	W
PAE	Max Power Added Efficiency	50	55	-	%
G _{PAE_MAX}	Associated Gain at Max PAE		12	-	dB

RF Characteristics (Pulsed)T_{case}= +25°C, Pulse mode ⁽¹⁾, F = 4GHz, V_{DS}=50V, I_{D_Q}=200mA

Symbol	Parameter	Min	Typ	Max	Unit
G _{SS}	Small Signal Gain	15	17		dB
P _{SAT}	Saturated Output Power	30	38		W
PAE	Max Power Added Efficiency	55	60		%
G _{PAE_MAX}	Associated Gain at Max PAE		13		dB

⁽¹⁾ Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between RF and DC pulse.

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB.

The typical performance achievable in more than 20% frequency band around 4GHz was demonstrated using the reference board 61500252 presented hereafter.

Absolute Maximum Ratings ⁽¹⁾T_{case}= +25°C^{(1), (2), (3)}

Symbol	Parameter	Rating	Unit	Note
V _{DS}	Drain-Source Voltage	60	V	
V _{GS_Q}	Gate-Source Voltage	-10, +2	V	⁽⁶⁾
I _{G_MAX}	Maximum Gate Current in forward mode	48	mA	
I _{G_MIN}	Maximum Gate Current in reverse mode	-8	mA	
I _{D_MAX}	Maximum Drain Current	4	A	⁽⁴⁾
P _{IN}	Maximum Input Power (typical)	37	dBm	⁽⁵⁾
T _j	Junction Temperature	220	°C	
T _{STG}	Storage Temperature	-55 to +150	°C	
T _{Case}	Case Operating Temperature	See note	°C	⁽⁴⁾

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

⁽³⁾ The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

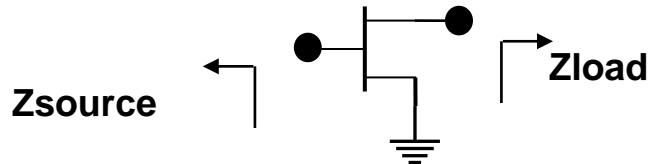
⁽⁴⁾ Max junction temperature must be considered

⁽⁵⁾ @4GHz -Linked to and limited by I_{G_MAX} & I_{G_MIN} values

⁽⁶⁾ V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values

Simulated Source and Load Impedance

$V_{DS} = 50V$, $I_{D_Q} = 200mA$



Frequency (MHz)	Source	Load
1000	$4.3 + j4$	$10.9 + j22.45$
2000	$1.5 - j1.5$	$7.2 + j10.7$
3000	$2.7 - j4.65$	$4.8 + j1.01$
4000	$3.9 - j8.6$	$4.27 - j0.38$
4500	$6.4 - j11$	$3.44 - j1.87$
5000	$7.8 - j3.2$	$2.5 - j3.8$

These values are given in the reference plane defined by the connection between the package leads and the PCB. A gap of 200 μ m is considered between the edge of the package and the PCB.

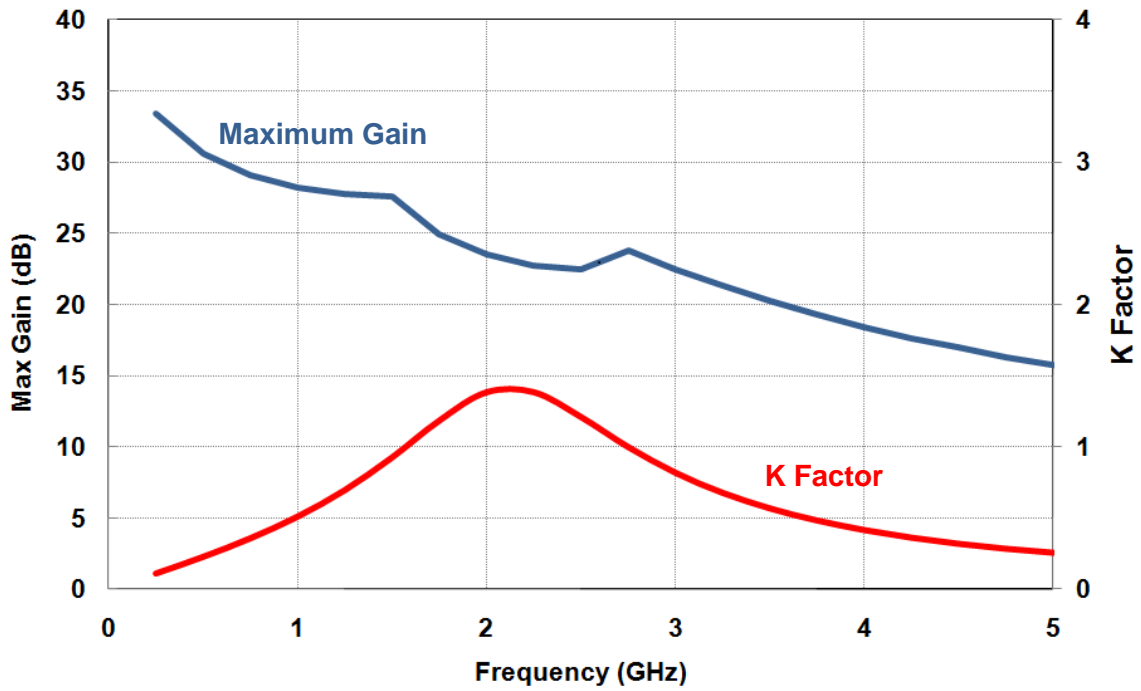
Typical S-parameters

T_{case}= +25°C, CW mode, V_D=50V, I_{D_Q}=200mA, Phase S(i,j) in °

Freq (GHz)	Mag S(1,1)	Phase S(1,1)	Mag S(2,1)	Phase S(2,1)	Mag S(1,2)	Phase S(1,2)	Mag S(2,2)	Phase S(2,2)
0.25	0.889	-129.151	31.653	105.909	0.014	19.700	0.372	-87.024
0.75	0.874	-154.710	16.399	84.547	0.014	2.237	0.374	-108.185
1.00	0.877	-164.553	10.726	71.530	0.013	-6.213	0.435	-117.969
1.25	0.884	-170.257	7.777	61.159	0.012	-10.890	0.503	-125.330
1.50	0.892	-174.377	5.973	52.235	0.010	-12.239	0.568	-131.757
1.75	0.900	-177.766	4.764	44.330	0.008	-9.485	0.625	-137.569
2.00	0.907	179.222	3.908	37.224	0.007	-1.247	0.673	-142.867
2.25	0.913	176.421	3.277	30.773	0.006	12.978	0.713	-147.712
2.50	0.918	173.741	2.800	24.861	0.006	29.717	0.747	-152.160
2.75	0.922	171.128	2.432	19.397	0.007	43.243	0.774	-156.264
3.00	0.925	168.546	2.143	14.298	0.009	51.631	0.797	-160.072
3.25	0.927	165.966	1.913	9.500	0.011	56.052	0.815	-163.632
3.50	0.928	163.363	1.730	4.942	0.013	57.956	0.830	-166.984
3.75	0.928	160.714	1.582	0.571	0.015	58.313	0.843	-170.164
4.00	0.928	157.996	1.462	-3.660	0.017	57.697	0.853	-173.204
4.25	0.927	155.184	1.365	-7.795	0.020	56.444	0.861	-176.134
4.50	0.925	152.254	1.288	-11.874	0.022	54.750	0.868	-178.979
4.75	0.922	149.175	1.226	-15.939	0.025	52.730	0.873	178.235
5.00	0.919	145.914	1.178	-20.028	0.027	50.453	0.876	175.487
5.25	0.915	142.433	1.142	-24.182	0.030	47.951	0.879	172.754
5.50	0.910	138.685	1.116	-28.445	0.033	45.238	0.881	170.016
5.75	0.904	134.617	1.101	-32.863	0.037	42.306	0.882	167.249
6.00	0.896	130.161	1.096	-37.488	0.040	39.135	0.882	164.430
6.25	0.888	125.236	1.100	-42.378	0.045	35.689	0.881	161.535
6.50	0.877	119.743	1.113	-47.599	0.049	31.919	0.880	158.535
6.75	0.865	113.560	1.136	-53.227	0.054	27.759	0.878	155.399
7.00	0.850	106.535	1.168	-59.352	0.060	23.129	0.875	152.088
7.25	0.834	98.485	1.209	-66.072	0.066	17.933	0.872	148.552
7.50	0.814	89.192	1.260	-73.499	0.073	12.056	0.868	144.729
7.75	0.793	78.408	1.320	-81.754	0.081	5.376	0.865	140.532
8.00	0.770	65.883	1.386	-90.953	0.090	-2.234	0.862	135.838
8.25	0.748	51.417	1.455	-101.199	0.100	-10.887	0.859	130.473
8.50	0.731	34.973	1.523	-112.557	0.110	-20.664	0.856	124.191
8.75	0.721	16.818	1.582	-125.041	0.119	-31.598	0.855	116.657
9.00	0.724	-2.382	1.625	-138.607	0.128	-43.670	0.852	107.445
9.25	0.741	-21.670	1.644	-153.180	0.135	-56.831	0.847	96.044
9.50	0.771	-40.101	1.636	-168.690	0.140	-71.043	0.838	81.883
9.75	0.809	-57.059	1.593	-174.919	0.142	-86.293	0.824	64.405
10.00	0.850	-72.322	1.511	-157.746	0.140	-102.524	0.809	43.293

Maximum Gain & Stability Characteristics

T_{case}= +25°C, CW mode, V_D=50V, I_{D_Q}=200mA

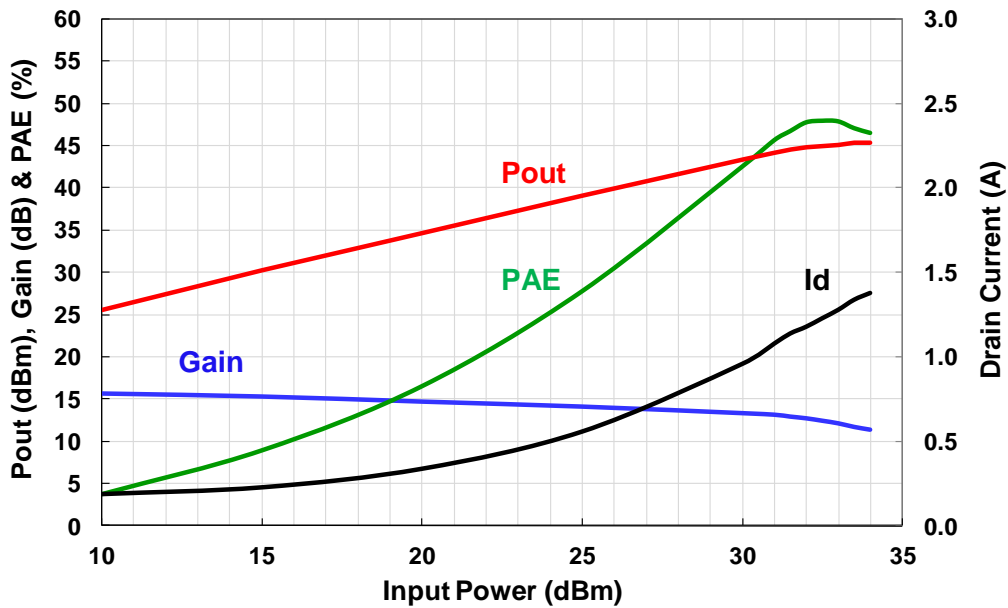


Typical Performance on Demonstration Board (Ref. 61500252)

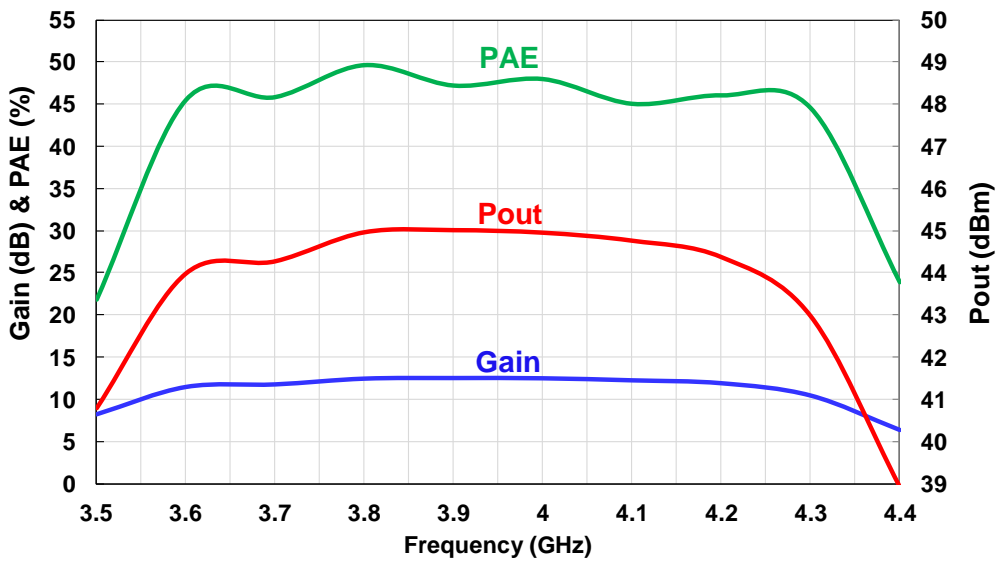
Calibration and measurements are done on the connector reference accesses of the demonstration boards.

T_{case} = +25°C, CW mode

Measured Pout, Gain, PAE & Id
 F = 4GHz, V_{DS} = 50V, I_{D,Q} = 200mA



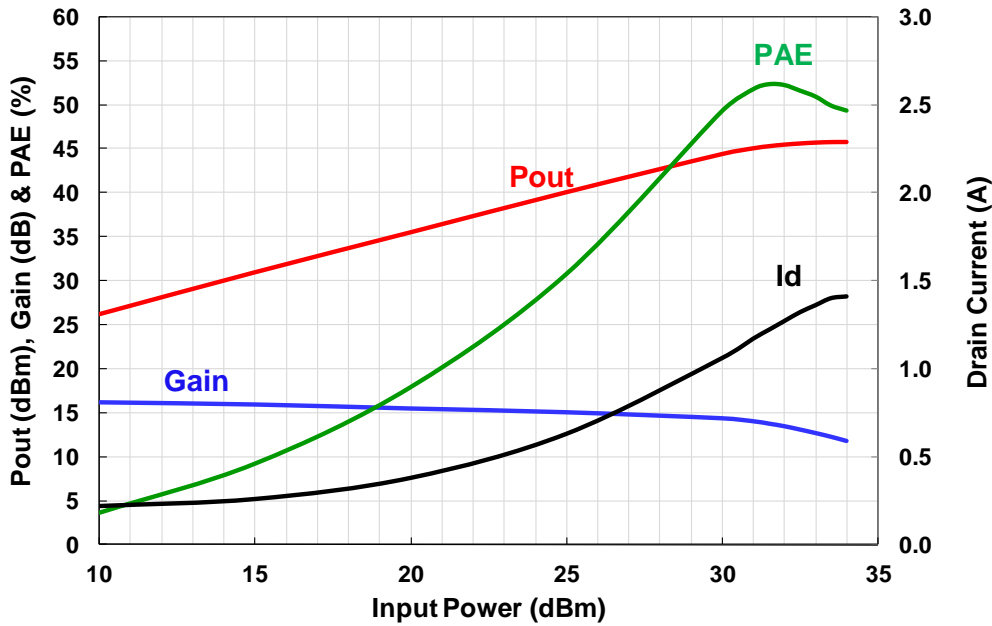
Measured Pout, PAE & Gain
 Pin = 32.5 dBm, V_{DS} = 50V, I_{D,Q} = 200mA



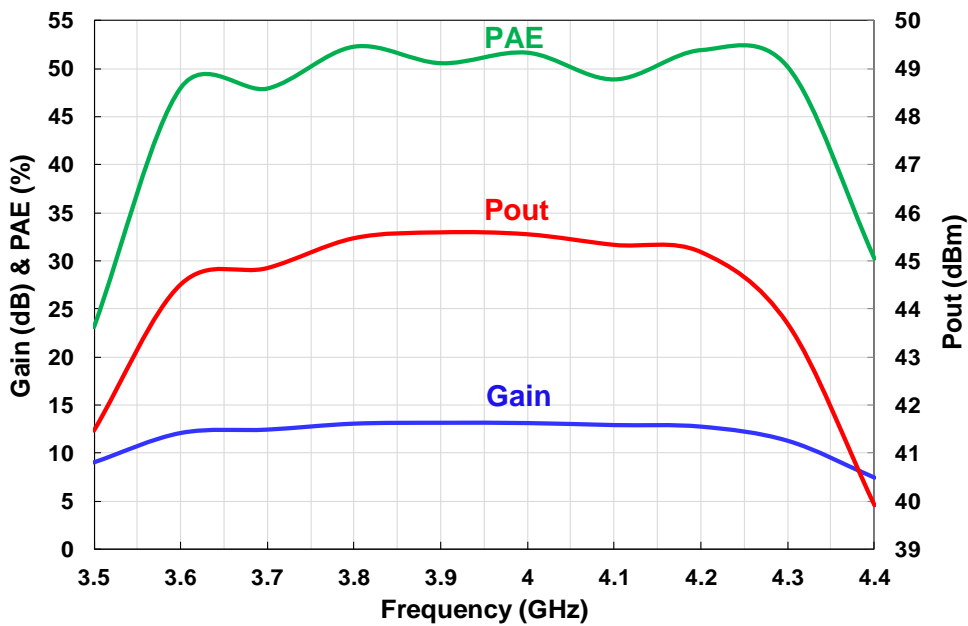
Typical Performance on Demonstration Board (Ref. 61500252)

Calibration and measurements are done on the connector reference accesses of the demonstration boards.

T_{case} = +25°C, Pulsed mode ⁽¹⁾
 Measured P_{out}, Gain, PAE & I_d
 F = 4GHz, V_{DS} = 50V, I_{D,Q} = 200mA



Measured P_{out}, PAE & Gain
 P_{in} = 32.5 dBm, V_{DS} = 50V, I_{D,Q} = 200mA



⁽¹⁾ Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between RF and DC pulse.

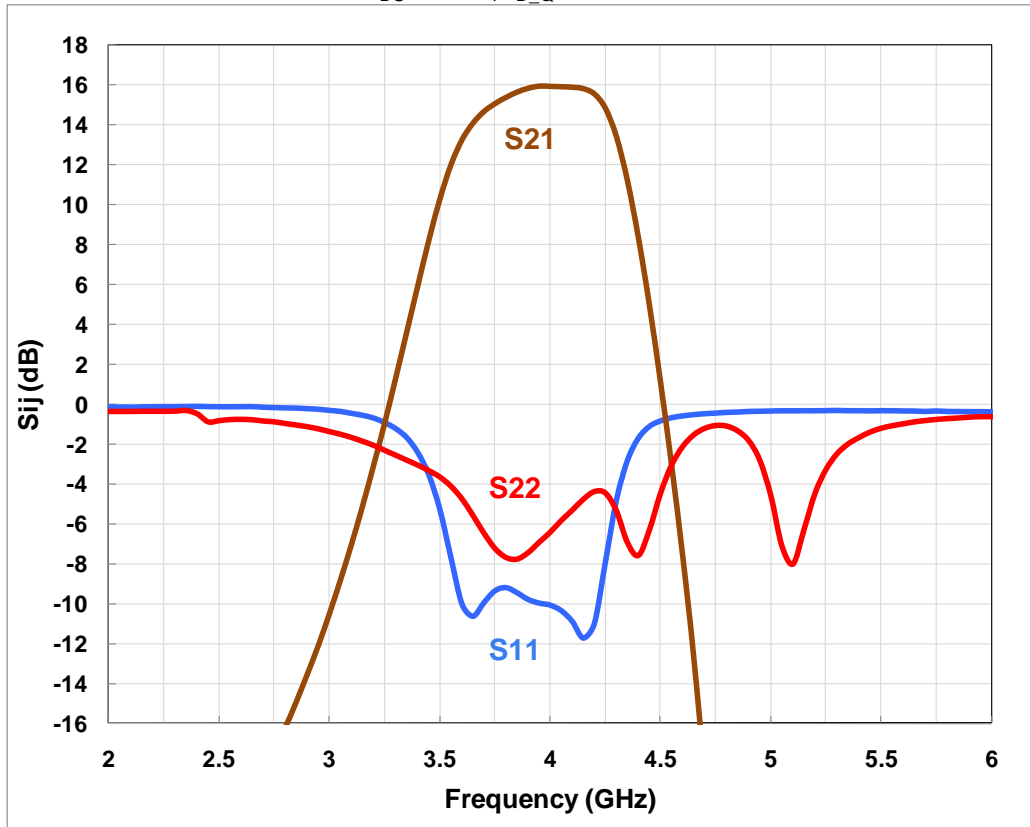
Typical Performance on Demonstration Board (Ref. 61500252)

Calibration and measurements are done on the connector reference accesses of the demonstration boards

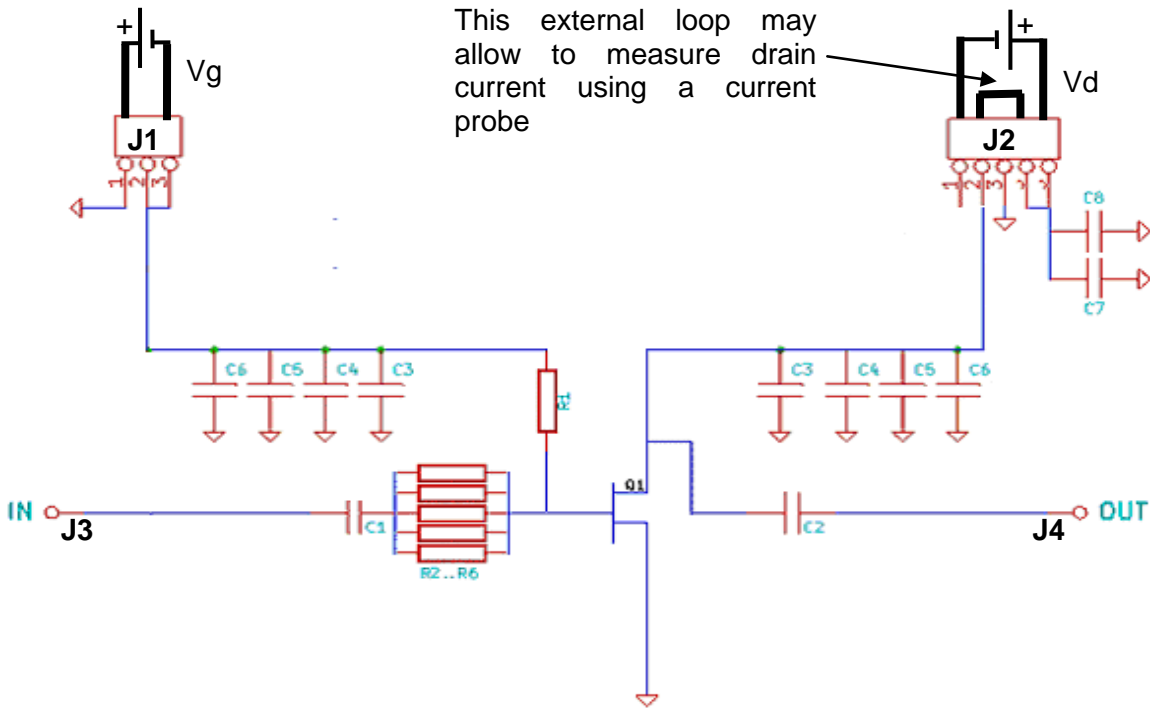
T_{case} = +25°C, CW mode

Measured S parameters

V_{DS} = 50V, I_{D_Q} = 200mA



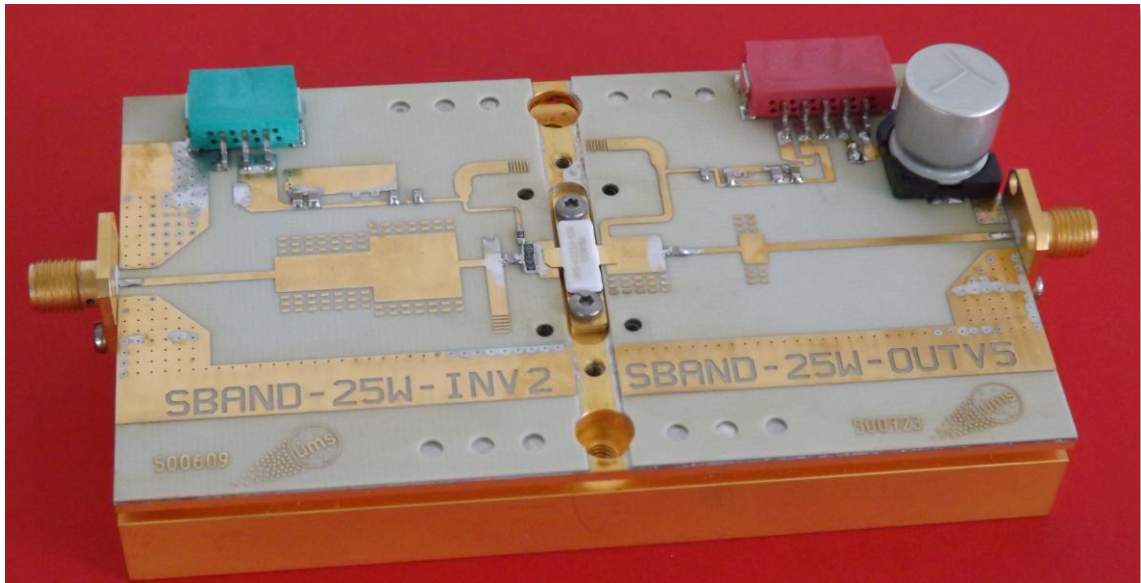
Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61500252)



Demonstration Amplifier (Ref. 61500252) / Bill of Materials

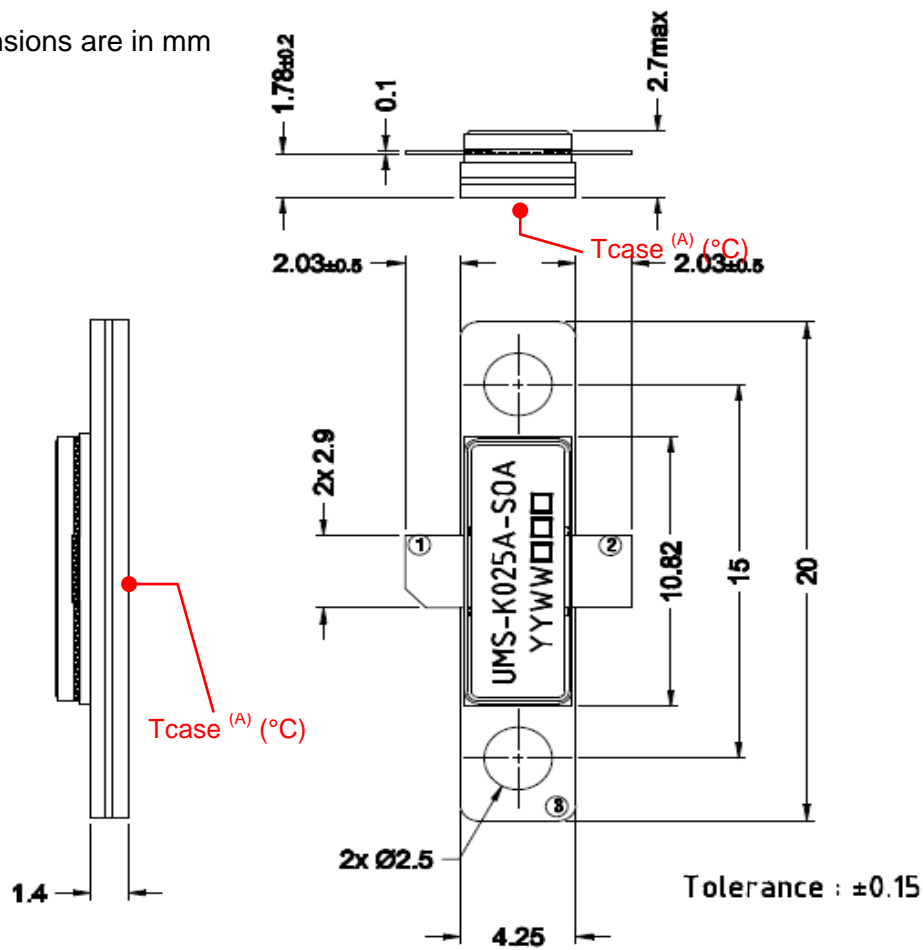
Designator	Type	Value - Description	Qty
C1	Capacitor	0.4pF, +/- 0.05pF, 0603	1
C2	Capacitor	0.6pF, +/- 0.05pF, 0603	1
C3	Capacitor	8.2pF, +/- 0.25%, 0603	2
C4	Capacitor	82pF, +/- 5%, 0603	2
C5	Capacitor	1nF, +/- 5%, 0805	2
C6	Capacitor	10nF, +/- 5%, 0805	2
C7	Capacitor	1µF, +/- 10%, 1204	1
C8	Capacitor	68µF, +/- 10%, 1204	1
R1	Resistor	147Ω, +/- 1%, 0603	1
R2..R6	Resistor	5,6Ω +/- 1%, 0603	5
J1	Connector	CMS 3cts	1
J2	Connector	CMS 5cts	1
J3,J4	Connector	SMA	2
Q1	Packaged Transistor	CHK025A-SOA	1
-	PCB	RO4003, Er=3.55, h= 508µm	-

Demonstration Amplifier Circuit (Ref. 61500252)



Package outline

All dimensions are in mm



PIN-OUT : 1- GATE
2- DRAIN
3- SOURCE (Gnd)

^(A) T_{case} locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design. Chamfered lead indicates the gate access of the packaged transistor.

Recommended Assembly Procedure

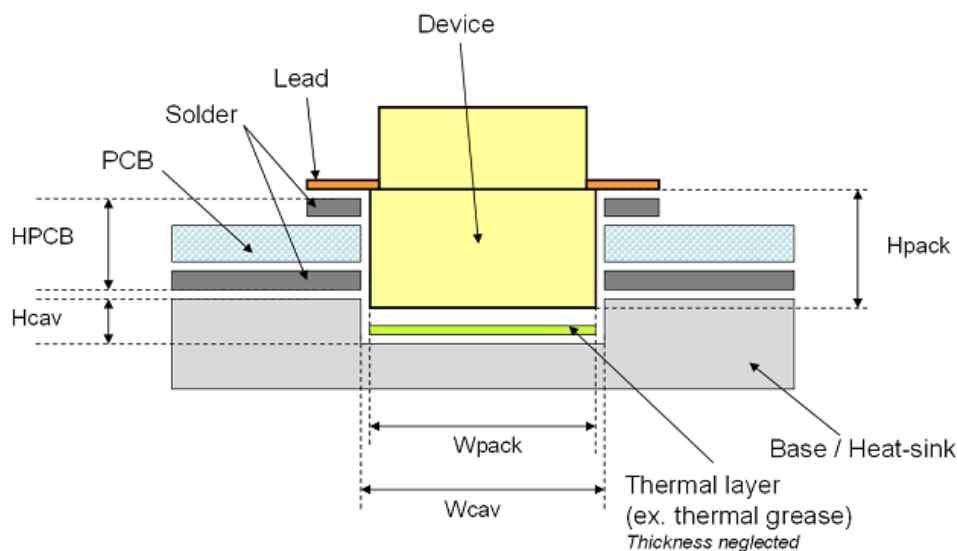
CHK025A-SOA is available has a flange package to be bolt down onto a thermal heat sink also used as main electrical ground. Use preferably screw M2 and flat washers.

Thermal and electrical resistance at the package to heat sink interface has to be as low as possible. Thermal electrically conductive grease or conductive thin layer like indium sheets are recommended between the package and the heat sink.

In case a thermal grease is selected, we recommend to use material offering thermal conductivity $>5\text{W/m.K}$ and electrical resistivity $<0.01\text{ ohm.cm}$. The grease layer thickness should be about $25\mu\text{m}$ (1 mil).

Contact interface quality can be improved by cleaning process prior device mounting on the heat-sink. Such operation will enhance the thermal and electrical contact by oxides removal at each interface.

Package leads can be soldered on printed circuit board's traces by using RoHS solder past. Cavity depth and width to be performed into the heat-sink where the device will be mounted are important to achieve the best performances. These dimensions have to be optimized in order to minimize the distance between device and signal traces made on the printed circuit board (PCB). But they also have to be calculated in order to accommodate device variations in height. The following drawing gives the relationship between device dimensions (H_{pack} & W_{pack}) and optimal cavity depth (H_{cav}) and width (W_{cav}) depending on the printed circuit-board configuration (HPCB)



$$H_{\text{cav}} = (H_{\text{pack}_{\text{min}}} - H_{\text{PCB}_{\text{max}}})^{+0}_{-0.05}$$

$$W_{\text{cav}} = (W_{\text{pack}_{\text{max}}} + 0.4) \pm 0.05$$

dimensions are in mm

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Package: CHK025A-SOA/XY
Tray: XY = 26

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